DLP® DLPA200 DMD Micromirror Driver

Check for Samples: DLPA200

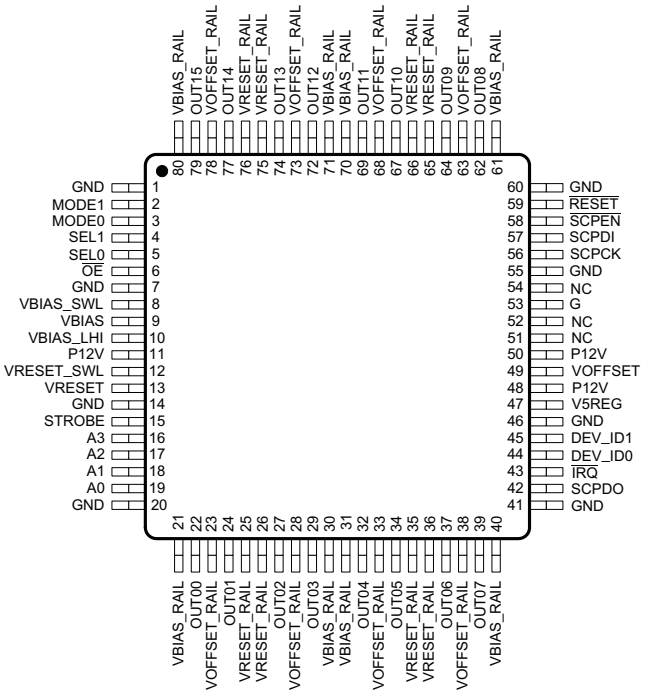
FEATURES

- **Designed for Use as a Part of a DLP Chipset**
- **Generates the Micromirror Clocking Pulses Required by the DLP Digital Micromirror Device (DMD)**
- **Generates Specialized Voltage Levels Required for Micromirror Clocking Pulse Generation**
- **Operates From a Single 12-V Power Supply**
- **Provides a V_{BIAS} Voltage Level, Used by the DMD to Control the Array Border Mirrors**
- **Provides a V_{OFFSET} Voltage Level, Used by the DMD as DMDVCC2**
- **All Logic Inputs are LVTTL and CMOS Compatible**
- **Packaged in an Pb-Free Thermally Enhanced Surface-Mount Package: 80-pin, 0.5 mm-Pitch, Enlarged Terminal Pitch, Thin Profile Quad Flat Pack (eTQFP)**

APPLICATIONS

- **Industrial:**
  - **Direct Imaging Lithography**
  - **Laser Marking and Repair Systems**
  - **Computer-to-Plate Printers**
  - **Rapid Prototyping Machines and 3D Printers**
  - **3D Scanners for Machine Vision and Quality Control**
- **Medical:**
  - **Phototherapy Devices**
  - **Ophthalmology**
  - **Vascular Imaging**
  - **Hyperspectral Imaging**
  - **3D Scanners for Limb and Skin Measurement**
  - **Confocal Microscopes**
- **Display:**
  - **3D Imaging Microscopes**
  - **Intelligent and Adaptive Lighting**
  - **Augmented Reality and Information Overlay**

ETQFP PACKAGE
(TOP VIEW)



DESCRIPTION

The DLPA200 is a DMD Micromirror Driver that is one of multiple components in a DLP chipset. A dedicated DLP chipset provides developers easier access to the DMD as well as high speed micromirror control.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION CONTINUED

Table 1 is a list of chipsets supported by DLPA200.

Table 1. Supported DLP Chipset Configurations

0.55 XGA Chipset			0.7 XGA Chipset			0.95 1080p Chipset		
Qty	TI Part	Description	Qty	TI Part	Description	Qty	TI Part	Description
1	DLP5500	0.55 XGA S450 DMD(digital micromirror device)	1	DLP7000	0.7 XGA Type A DMD(digital micromirror device)	1	DLP9500	0.95 1080p Type A DMD(digital micromirror device)
1	DLPC200	DMD Controller for DLP5500	1	DLPC410	DLP Discovery 4100 DMD Controller	1	DLPC410	DLP Discovery 4100 DMD Controller
			1	DLPR410	DLP Discovery 4100 Configuration PROM	1	DLPR410	DLP Discovery 4100 Configuration PROM
1	DLPA200	DMD Micromirror Driver	1	DLPA200	DMD Micromirror Driver	2	DLPA200	DMD Micromirror Driver

Reliable function and operation of the DLPA200 requires that it be used in conjunction with the other components of the chipset. It is typical for the DMD Controller to operate the DMD Micromirror Driver. For mor information on the chipset components the DLP 0.55 XGA Chipset Datasheet or DLP Discovery 4100 Chipset Datasheet.

The DLPA200 consists of three functional blocks: A High-Voltage Power Supply function, a DMD Micromirror Clock Generation function, and a Serial Communication function.

The High-Voltage Power Supply function generates three specialized voltage levels: V_{BIAS} (19 to 28 V), V_{RESET} (–19 to –28 V), and V_{OFFSET} (4.5 to 10 V).

The Micromirror Clock Generation function uses the three voltages generated by the High-Voltage Power Supply function to create the sixteen micromirror clock pluses (output the OUTx pins of the DLPA200).

The Serial Communication function allows the chipset Controller to: control the generation of V_{BIAS}, V_{RESET}, and V_{OFFSET}; control the generation of the micromirror clock pulses; status the general operation of the DLPA200.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Functional Block Diagram

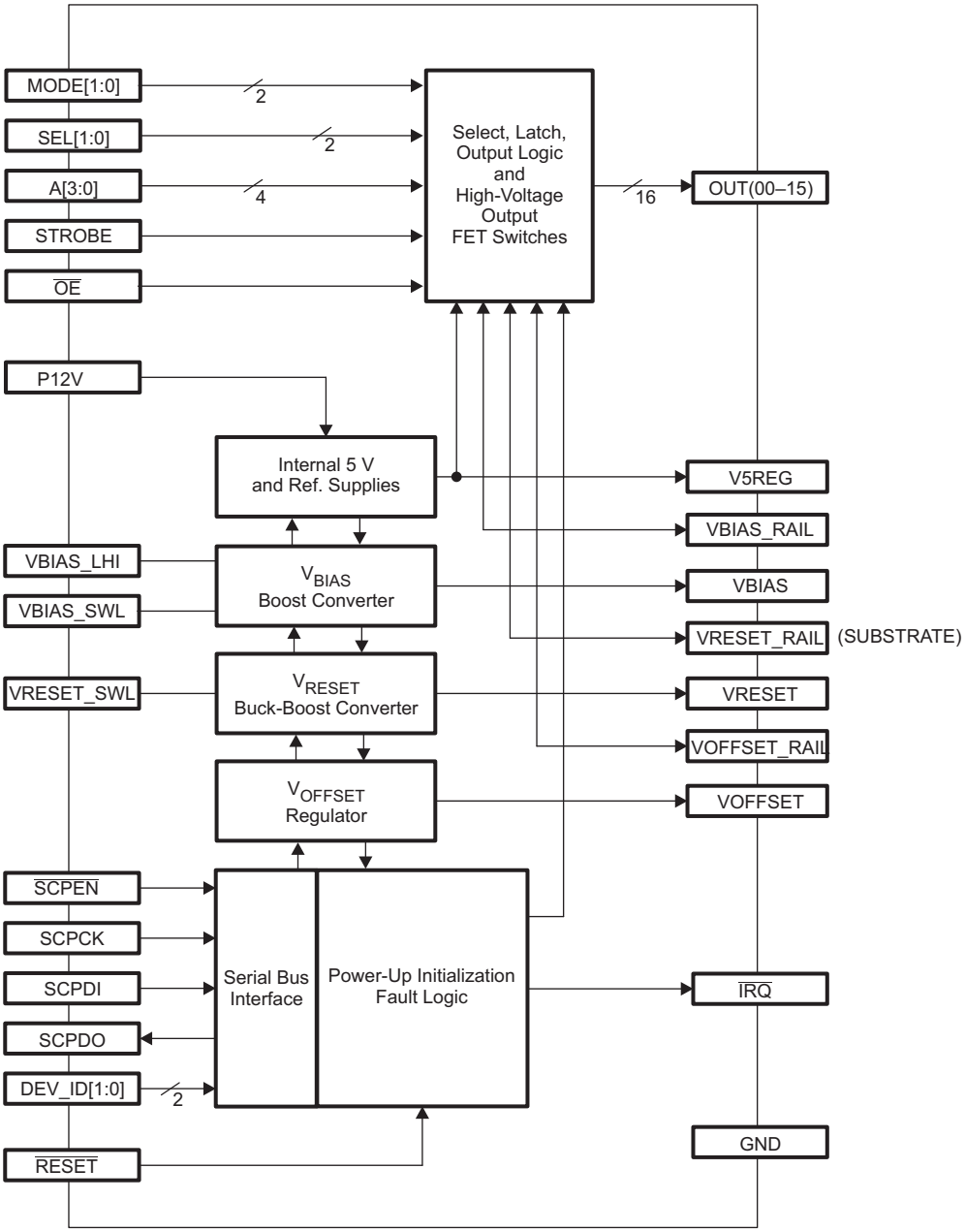


Table 2. Device Configurations

DMD	POWER AND MIRROR CLOCKING PULSE DRIVER	DIGITAL CONTROLLER
DLP9500 (0.95 1080p Type A DMD)	DLPA200 (x2)	DLPC410
DLP7000 (0.7 XGA Type A DMD)	DLPA200	
DLP5500 (0.55 XGA S450 DMD)	DLPA200	DLPC200

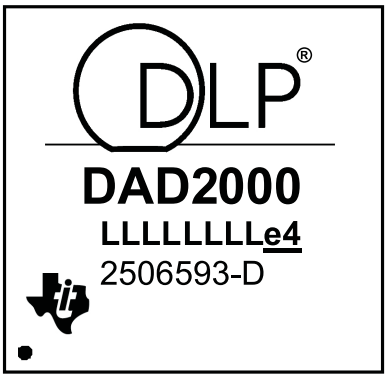
RELATED DOCUMENTS

Table 3. Related Documentation

Document	TI Literature Number
DLP 0.55 XGA Chip-Set data sheet	DLPZ004
DLP5500 0.55 XGA DMD data sheet	DLPS013B
DLPC200 Digital Controller data sheet	DLPS014
DLP® Discovery™ 4100 Chipset Datasheet	DLPU008
DLP7000 0.7 XGA Type-A DMD data sheet	DLPS026
DLP9500 0.95 1080p Type-A DMD data sheet	DLPS025
DLPC410 Digital Controller data sheet	DLPS024
DLPA200 DMD Micromirror Driver data sheet	DLPS015
DLPR410 EEPROM data sheet	DLPS027

Device Marking

The device marking consists of the fields shown in Figure 1.



PART MARKING CODES

LLLLLLLL = Lot trace code or date code

e4 = Pb-Free NiPdAu terminal finish

● = Pin 1 designator

2506593 = TI internal part number

D = revision letter

Figure 1. Device Marking (Device Top View)

DLPA200PFC is functionally equivalent to 2506593-0005N.

TERMINAL FUNCTIONS

TERMINAL		I/O (INPUT DEFAULT)	DESCRIPTION
NAME	NO.		
OUT00	22	Output	16 micromirror clocking waveform outputs (enabled by $\overline{OE}$ = 0).
OUT01	24	Output	
OUT02	27	Output	
OUT03	29	Output	
OUT04	32	Output	
OUT05	34	Output	
OUT06	37	Output	
OUT07	39	Output	
OUT08	62	Output	
OUT09	64	Output	
OUT10	67	Output	
OUT11	69	Output	
OUT12	72	Output	
OUT13	74	Output	
OUT14	77	Output	
OUT15	79	Output	
A0	19	Input (pull down)	Output Address. Used to select which OUTxx pin is active at a given time.
A1	18	Input (pull down)	
A2	17	Input (pull down)	
A3	16	Input (pull down)	
MODE0	3	Input (pull down)	Mode Select. Used to determine the operating mode of the DLPA200.
MODE1	2	Input (pull down)	
SEL0	5	Input (pull down)	Output Voltage Select. Used to switch the voltage applied to the addressed OUTxx pin.
SEL1	4	Input (pull down)	
STROBE	15	Input (pull down)	A rising edge on STROBE latches in the control signals after a tri-state delay.
$\overline{OE}$	6	Input (pull up)	Asynchronous input controls whether the 16 OUTxx pins are active or are in a in high-impedance state. $\overline{OE}$ = 0 : Enabled. $\overline{OE}$ = 1 : High Z.
$\overline{RESET}$	59	Input (pull up)	Resets the DLPA200 internal logic. Active low. Asynchronous.

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O (INPUT DEFAULT)	DESCRIPTION
NAME	NO.		
$\overline{\text{SCPEN}}$	58	Input (pull up)	Enables serial bus data transfers. Active low.
SCPDI	57	Input (pull down)	Serial bus data input. Clocked in on the falling edge of SCPCK.
SCPCK	56	Input (pull down)	Serial bus clock. Provided by chipset Controller.
SCPDO	42	Output	Serial bus data output (open drain). Clocked out on the rising edge of SCPCK. A 1kΩ pull up resistor to the Chip-Set Controller V_{DD} supply is recommended.
$\overline{\text{IRQ}}$	43	Output	Interrupt request output to the chipset Controller. Active low. A 1 kΩ pull up resistor to the Chip-Set Controller V_{DD} supply is recommended.
DEV_ID1	45	Input (pull up)	Serial bus device address: 00 = all; 01 = device 1; 10 = device 2; 11 = device 3.
DEV_ID0	44	Input (pull up)	
VBIAS	9	Output	One of three specialized voltages which are generated by the DLPA200.
VBIAS_LHI	10	Input	Current limiter output for VBIAS supply. (also the VBIAS switching inductor input)
VBIAS_SWL	8	Input	Connection point for VBIAS supply switching inductor.
VBIAS_RAIL	21, 30, 31, 40, 61, 70, 71, 80	Input	The internally-used VBIAS supply rail. Internally isolated from VBIAS.
VRESET	13	Output	One of three specialized voltages which are generated by the DLPA200. The package thermal pad is tied to this voltage level.
VRESET_SWL	12	Input	Connection point for VRESET supply switching inductor..
VRESET_RAIL(1)	25, 26, 35,36, 65, 66, 75, 76	Input	The internally-used VRESET supply rail. Internally isolated from VRESET.(1)
VOFFSET	49	Output	One of three specialized voltages which are generated by the DLPA200.
VOFFSET_RAIL	23, 28, 33, 38, 63, 68, 73, 78	Input	The internally-used VOFFSET supply rail. Internally isolated from VOFFSET.
GND	1, 7, 14, 20, 41, 46, 53, 55, 60	GND	Common ground
V5REG	47	Output	The 5-volt logic supply output.
P12V	11, 48, 50	Input	The main power input to the DLPA200.
NC	51, 52, 54	No Connect	No connect

(1) Exposed thermal pad is internally connected to VRESET_RAIL.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. The Absolute Maximum Ratings are stress ratings only, and functional performance of the device at these or any other conditions beyond those indicated under " Recommended Operating Conditions" is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

CONDITIONS		MIN	TYP	MAX	UNIT
Load supply voltage, P12V				14	V
Reset supply switching inductor connection point, VRESET_SWL	Measured with respect to VRESET_RAIL			–1	V
Internally-used V_{BIAS} supply rail, VBIAS_RAIL	Measured with respect to VRESET_RAIL			60	V
Internally-used V_{OFFSET} supply rail, VOFFSET_RAIL	Measured with respect to VRESET_RAIL			40.5	V
Logic inputs, V_{IN}		–0.3		7	V
Open drain logic outputs, V_{OUT}				7	V
Maximum junction temperature, T_J				125	°C
Operating temperature range, T_A		0		75	°C
Storage temperature range, T_S		–55		150	°C
Thermal resistance, R_{c-j}	V_{BIAS} = 26 V, V_{RESET} = -26 V, V_{OFFSET} = 10 V, Output load = 390 pF and 39R on each output, Phase by one with global mode, Channel repetition frequency = 50 kHz, Additional external loads: I_{BIAS} = 5 mA, I_{OFFSET} = 30 mA, I_{5REG} = 30 mA		3		°C/W
ESD	Human Body Model			2	kV
	Charge Device Model			800	V

RECOMMENDED OPERATING CONDITIONS

at T_A = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power						
I_{P12V1}	P12V supply current(1)	Global shadow at 50 kHz, OUT load = 39 Ω and 390 pF, V5REG = 30 mA, V_{BIAS} = 26 V at 5 mA, V_{OFFSET} = 10V at 30 mA, V_{RESET} = –26 V		200		mA
I_{P12V2}		Outputs disabled and no external loads, V_{BIAS} = 19 V, V_{OFFSET} = 4.5 V, V_{RESET} = –19 V			22	mA
T_{JTSDR}	Thermal shutdown temperature	With device temperature rising	145	160	175	°C
		Hysteresis	5	10	15	°C
	Delta between thermal shutdown and thermal warning		5	10	15	°C
T_{JTWR}	Thermal warning temperature	With device temperature rising	125	140	155	°C
		Hysteresis	5	10	15	°C

(1) During power up the inrush power supply current can be as high as 1 A for a momentary period of time.

ELECTRICAL CHARACTERISTICS
Control Logic

T_A = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low-level logic input voltage				0.8	V
V_{IH}	High-level logic input voltage		1.97			V
I_{IH}	High-level logic input current	V_{IN} = 5 V, input with pulldown. See terminal functions table.		40	50	µA
I_{IL}	Low-level logic input current	V_{IN} = 0 V, input with pullup. See terminal functions table.	–50	–40		µA
I_{IH}	High-level logic input leakage current	V_{IN} = 0 V, input with pulldown	–1		1	µA
I_{IL}	Low-level logic input leakage current	V_{IN} = 5 V, input with pullup	–1		1	µA
V_{OL}	Open drain logic outputs	I = 4 mA			0.4	V
I_{OL}	Logic output leakage current	V = 3.3 V			1	µA

ELECTRICAL CHARACTERISTICS
5-V Linear Regulator

T_A = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{5REG}	Output voltage	Average voltage, I_{OUT} = 4 mA to 50 mA		4.75	5	5.25	V
I_{IL}	Output current: internal logic			4		20	mA
I_{IE}	Output current: external circuitry			0		30	mA
I_{CL5}	Current limit			80			mA
V_{UV5}	Undervoltage threshold	I_{OUT} = 50 mA	V5REG voltage increasing, P12V = 5.4 V		4.1		V
			V5REG voltage falling, P12V = 5.2 V		3.9		
V_{RIP}	Output ripple voltage(1)					200	mVpk-pk
V_{OS5}	Voltage overshoot at start up					2	%V5REG
t_{ss}	Power up	Measured between 10 to 90% of V5REG				1	ms

(1) Output ripple voltage relies on suitable external components being selected and good printed circuit board layout practice.

ELECTRICAL CHARACTERISTICS
Bias Voltage Boost Converter

T_A = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{RL}	Output current: reset outputs	Load = 400pF, 39 Ω, repetition frequency = 50 kHz	0		18	mA
I_{QL}	Output current: quiescent / drivers	Load = 400 pF, 39 Ω, r epetition frequency = 50 kHz			3	mA
I_{DL}	Output current: DMD load		0		5	mA
I_{CLFB}	Current limit flag	Corresponding current on output at P12V = 10.8 V	30			mA
I_{CLB}	Current limit	Measured on input	330	376	460	mA
V_{BIAS}	Output voltage		25.5	26	26.5	V
V_{UVB}	V_{BIAS} undervoltage threshold	Bias voltage falling	50		92	%VBIAS
V_{UVLHI}	VBIAS_LHI undervoltage threshold	VBIAS_LHI voltage increasing		8		V
		VBIAS_LHI voltage falling		6.5		V
R_{DS}	Boost switch $R_{DS(on)}$	T_J = 25°C		2		Ω
V_{RIP}	Output ripple voltage(1)				200	mVpk-pk
F_{SW}	Switching frequency		1.35	1.5	1.65	MHz
V_{OSB}	Voltage overshoot at start up				2	%VBIAS
t_{ss}	Power up	C_{OUT} = 3.3 µF, Measured between 10 to 90% of target V_{BIAS}			1	ms
t_{dis}	Discharge current sink		400			mA

(1) Output ripple voltage relies on suitable external components being selected and good printed circuit board layout practice.

ELECTRICAL CHARACTERISTICS
Reset Voltage Buck-Boost Converter

T_A = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{RL}	Output current: reset outputs	Load = 400 pF, 39 Ω, repetition frequency = 50 kHz	0		18	mA
I_{QL}	Output current: quiescent / drivers	Load = 400 pF, 39 Ω , repetition frequency = 50 kHz			3	mA
I_{CLFR}	Current limit flag	Corresponding current on output at P12V = 10.8 V	25			mA
I_{CLR}	Current limit	Measured on input	400		800	mA
V_{RESET}	Output voltage		-25.5	-26	-26.5	V
V_{UVR}	Undervoltage threshold	Reset voltage falling	50		92	%VRESET
R_{DS}	Buck-boost switch $R_{DS(on)}$	T_J = 25°C		8		Ω
V_{RIP}	Output ripple voltage(1)				200	mVpk-pk
F_{SW}	Switching frequency		1.35	1.5	1.65	MHz
V_{OSR}	Voltage overshoot at start up				2	%VRESET
t_{ss}	Power up	C_{OUT} = 3.3 µF, Measured between 10 to 90% of target V_{RESET}			1	ms
t_{dis}	Discharge current sink		400			mA

(1) Output ripple voltage relies on suitable external components being selected and good printed circuit board layout practice.

ELECTRICAL CHARACTERISTICS
V_{OFFSET}/DMDVCC2 Regulator

T_A = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{RL}	Output current: reset outputs	Load = 400 pF, 39 Ω, repetition frequency = 50 kHz	0		12.2	mA
I_{QL}	Output current: quiescent / drivers	Load = 400 pF, 39 Ω, repetition frequency = 50 kHz			3	mA
I_{DL}	Output current: DMDVCC2		0		30	mA
I_{CLO}	Current limit		100			mA
V_{OFFSET}	Output Voltage	DLP9500, DLP5500	8.25	8.5	8.75	V
		DLP7000	7.25	7.5	7.75	
V_{UVO}	Undervoltage threshold	V_{OFFSET} voltage falling	50		92	%VOFFSET
V_{RIP}	Output ripple voltage(1)				100	mVpk-pk
V_{OSO}	Voltage overshoot at start-up				2	%VOFFSET
t_{ss}	Power up	C_{OUT} = 4.7 µF, Measured between 10 to 90% of target V_{OFFSET}			1	ms
t_{dis}	Discharge time constant				100	µs

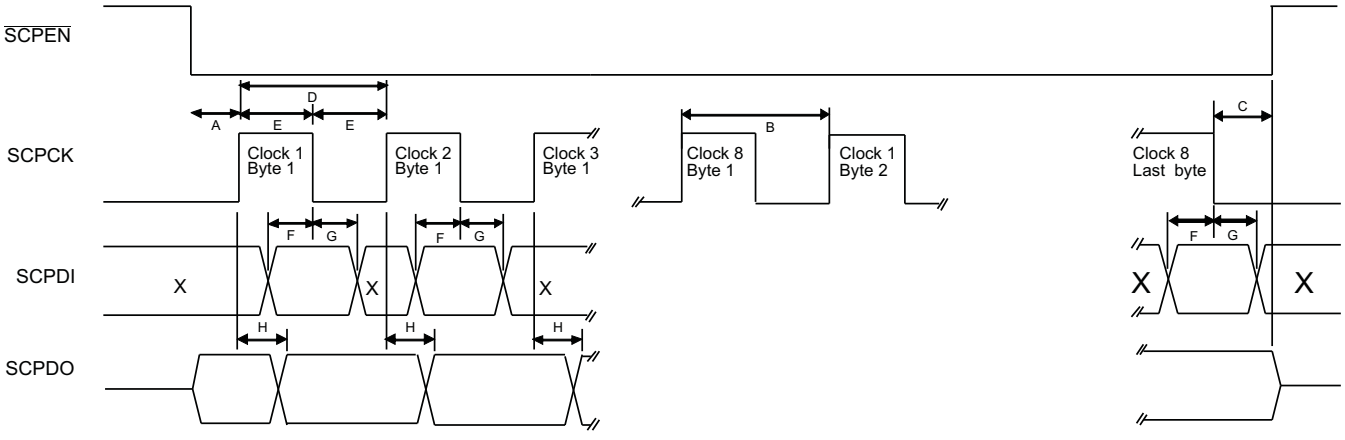
(1) Output ripple voltage relies on suitable external components being selected and good printed circuit board layout practice.

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Serial Communication Port Interface						
A(1)	Setup $\overline{\text{SCPEN}}$ Low To SCPCK	Reference to rising edge of SCPCK	360			ns
B(1)	Byte To Byte Delay	Nominally 1 SCPCK cycle, rising edge to rising edge	1.9			µs
C(1)	Setup SCPDI To $\overline{\text{SCPEN}}$ High	Last byte to slave disable	360			ns
D(1)	SCPCK Frequency(2)		0		526	kHz
	SCPCK Period		1.9	2		µs
E(1)	SCPCK High Or Low Time		300			ns
F(1)	SCPDI Set-Up Time	Reference to falling edge of SCPCK	300			ns
G(1)	SCPDI Hold Time	Reference from falling edge of SCPCK	300			ns
H(1)	SCPDO Propagation Delay	Reference from rising edge of SCPCK			300	ns
	$\overline{\text{SCPEN}}$, SCPCK, SCPDI, $\overline{\text{RESET}}$ Filter (Pulse Reject)		150			ns
Output Micromirror Clocking Pulses						
F_{PREP}	Phased reset repetition frequency each output pin (non-overlapping)				50	kHz
F_{GREP}	Global reset repetition frequency all output pins				50	kHz
I_{RLK}	V_{RESET} output leakage current	$\overline{\text{OE}}$ = 1, VRESET_RAIL = -28.5V		-1	-10	µA
I_{BLK}	V_{BIAS} output leakage current	$\overline{\text{OE}}$ = 1, VBIAS_RAIL = 28.5V		1	10	µA
I_{OLK}	V_{OFFSET} output leakage current	$\overline{\text{OE}}$ = 1, VOFFSET_RAIL = 10.25V		1	10	µA
Output Micromirror Clocking Pulse Controls						
t_{SPW}	STROBE Pulsewidth		10			ns
t_{SP}	STROBE Period		20			ns
t_{OHZ}	Output Time To High Impedance	$\overline{\text{OE}}$ Pin = High			100	ns
t_{OEN}	Output Enable Time From High Impedance	$\overline{\text{OE}}$ Pin = Low			100	ns
t_{SUS}	Set-Up Time	From A[3:0], MODE[1:0], and SEL[1:0] to STROBE edge	8			ns
t_{HOS}	Hold time	From A[3:0], MODE[1:0], and SEL[1:0] to STROBE edge	8			ns
t_{PBR}	Propagation time	From STROBE to V_{BIAS}/V_{RESET} edge 50% point.	80		200	ns
t_{PRO}		From STROBE to V_{RESET}/V_{OFFSET} edge 50% point.	80		200	ns
t_{POB}		From STROBE to V_{OFFSET}/V_{BIAS} edge 50% point.	80		200	ns
t_{DEL}	Edge-to-edge propagation delta	Maximum difference between the slowest and fastest propagation times for any given reset output.			40	ns
t_{CHCH}	Output channel-to-channel propagation delta	Maximum difference between the slowest and fastest propagation times for any two outputs for any given edge.			20	ns

(1) See Figure 2
(2) There is no minimum speed for the serial port. It can be written to statically for diagnostic purposes.



X = Don't care

Figure 2. Serial Interface Timing

PRINCIPLES OF OPERATION

5-V Linear Regulator

The 5-V linear regulator supplies the 5 V requirement of the DLPA200 internal logic.

Figure 3 shows the block diagram of this module. The input de-coupling capacitors are shared with other internal DLPA200 modules. See Component Selection Guidelines for recommended component values.

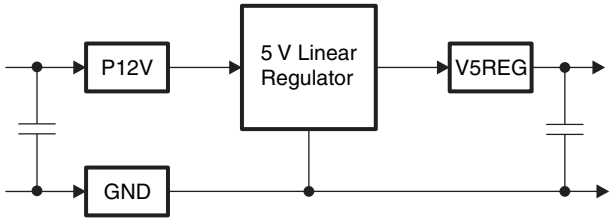


Figure 3. 5-Volt Linear Regulator Block Diagram

Bias Voltage Boost Converter

The bias voltage converter is a switching supply that operates at 1.5 MHz. The bias switching device switches 180° out-of-phase with the reset switching device.

The converter supplies the internal bias voltage for the high voltage FET switches and the external V_{BIAS} for the DMD border mirrors. The V_{BIAS} voltage level can be different for different generations of DMDs. The V_{BIAS} voltage level is configured by the DLP Controller chip over a serial communication interface. Four control bits select the voltage level while a fifth bit is the on/off control. The module provides two status bits to indicate latched and unlatched status bits for under-voltage (V_{UV}) and current-limit (C_L) conditions.

Figure 4 shows the block diagram of this module. The input de-coupling capacitors are shared with other internal DLPA200 modules. See Component Selection Guidelines for recommended component values.

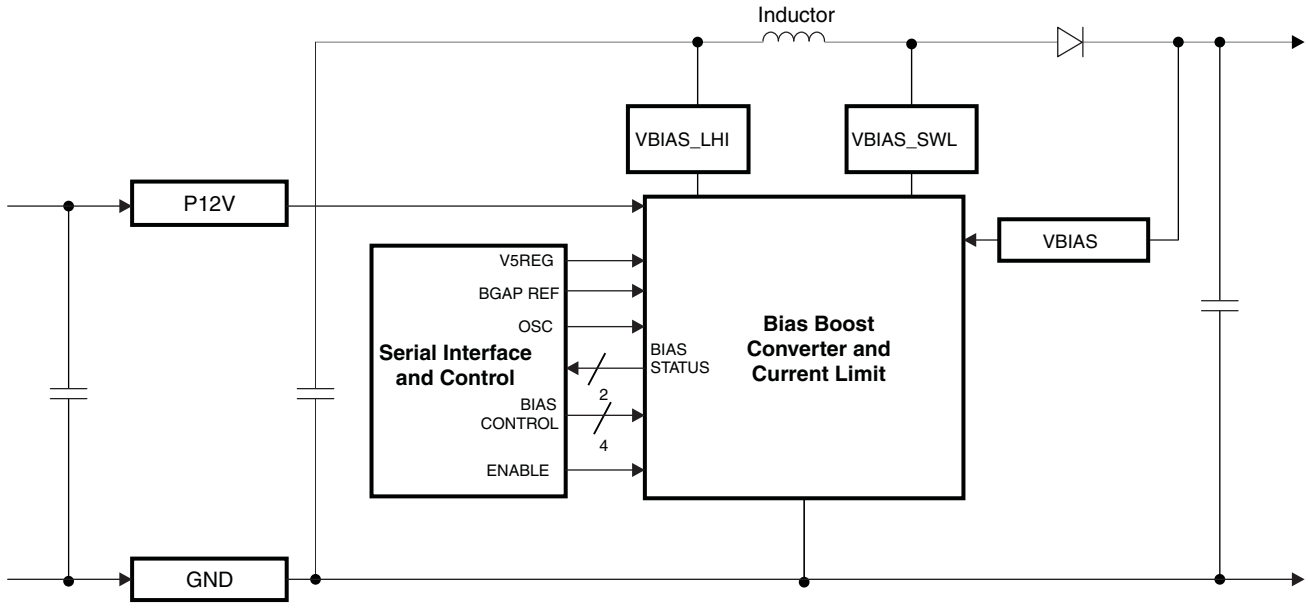


Figure 4. Bias Voltage Boost Converter Block Diagram

Reset Voltage Buck-Boost Converter

The reset voltage buck-boost converter is a switching supply that operates at 1.5 MHz. The reset switching device switches 180° out-of-phase with the bias switching device.

The converter supplies the internal reset voltage levels for the high voltage FET switches. The V_{RESET} voltage level can be different for different generations of DMDs. The V_{RESET} voltage level is configured by the DLP Controller chip over a serial communication interface. Four control bits select the voltage level while a fifth bit is the on/off control. The module provides two status bits to indicate latched and unlatched status bits for under-voltage (V_{UV}) and current-limit (C_L) conditions.

Figure 5 shows the block diagram of this module. The input de-coupling capacitors are shared with other internal DLPA200 modules. See Component Selection Guidelines for recommended component values.

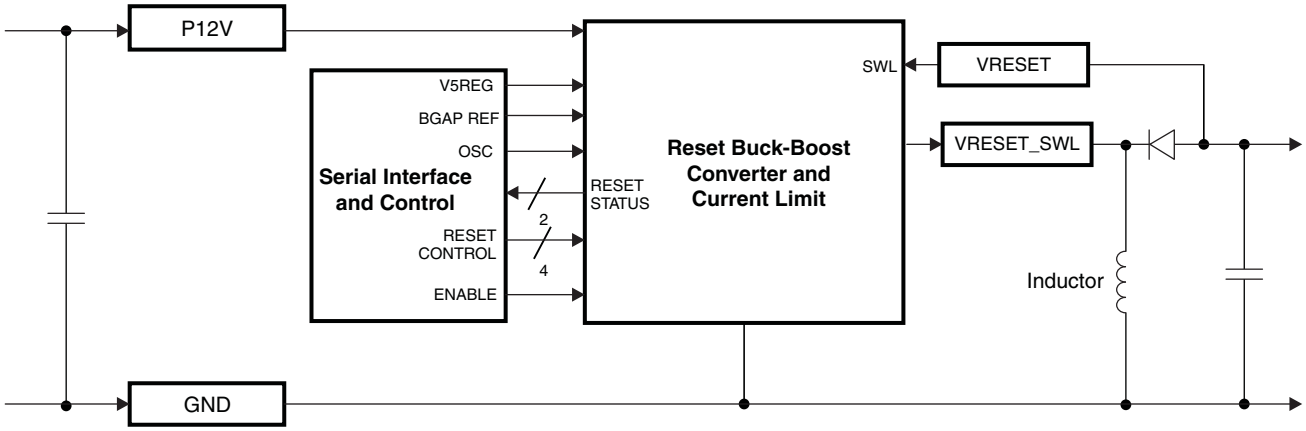


Figure 5. Reset Voltage Buck-Boost Converter Block Diagram

V_{OFFSET}/DMDVCC2 Regulator

The V_{OFFSET}/DMDVCC2 regulator supplies the internal V_{OFFSET} voltage for the high voltage FET switches and the external DMDVCC2 for the DMD. The V_{OFFSET} voltage level can be different for different generations of DMDs. The V_{OFFSET} voltage level is configured by the DLP Controller chip over a serial communication interface. Four control bits select the voltage level while a fifth bit is the on/off control. The module provides 2 status bits to indicate latched and unlatched status bits for under-voltage (V_{UV}) and current-limit (C_L) conditions.

Figure 6 shows the block diagram of this module. The input de-coupling capacitors are shared with other DLPA200 modules. See Component Selection Guidelines for recommended component values.

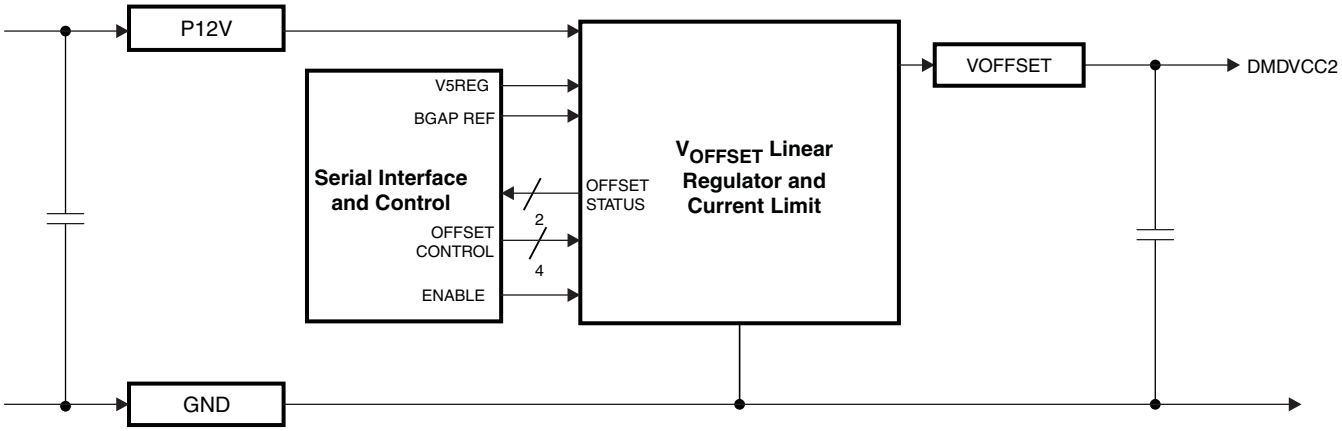


Figure 6. Offset Voltage Boost Convertor Block Diagram

Serial Communications Port (SCP)

The Serial Communications Port (SCP) is a full duplex, synchronous, character-oriented (byte) port that allows exchange of data between the master ASIC or FPGA, and one or more slave DAD2000s (and/or other DLPTM devices).

Table 4. Serial Communications Port Signal Definitions

SIGNAL	I/O	FROM/TO	TYPE	DESCRIPTION
SCPCK	I	SCP bus master to slave	LVTTL compatible	SCP bus serial transfer clock. The host processor (master) generates this clock.
$\overline{\text{SCPEN}}$	I	SCP bus master to slave	LVTTL compatible	SCP bus access enable (low true). When high, slave will reset to idle state, and SCPDO output will tri-state. Pulling $\overline{\text{SCPEN}}$ low initiates a read or write access. $\overline{\text{SCPEN}}$ must remain low for an entire read/write access, and must be pulled high after the last data cycle. To abort a read or write cycle, pull $\overline{\text{SCPEN}}$ high at any point.
SCPDI	I	SCP bus master to slave	LVTTL compatible	SCP bus serial data input. Data bits are valid and must be clocked in on the falling edge of SCPCK.
SCPDO	O	SCP bus slave to master	LVTTL, open drain w/tri-state	SCP bus serial data output. Data bits must clocked out on the rising edge of SCPCK. A 1k pull up resistor to the 3.3 volt ASIC supply is required.
$\overline{\text{IRQ}}$	O	SCP bus slave to master	LVTTL, open drain	Not part of the SCP bus definition. Asynchronous interrupt signal from slave to request service from master. A 1k pull up resistor to the 3.3 volt ASIC supply is required.

PWB LAYOUT AND ROUTING GUIDELINES

CAUTION

Board layout and routing guidelines must be followed explicitly and all external components used must be in the range of values and of the quality recommended for proper operation of the DLPA200. Important: Thermal pad(s) must be tied to VRESET_RAIL, do not connect to ground.

CAUTION

Thermal pad(s) must be tied to VRESET_RAIL, do not connect to ground.

General Guidelines

Suitable Kelvin connections should be provided for the switching regulator feedback pins: V_{BIAS} (pin 9) and V_{RESET} (pin 13).

The etch traces that connect the switching devices: VBIAS_SWL (pin 8) and VRESET_SWL (pin 12) should be as short and wide as possible to minimize leakage inductances. The etch traces that connect the switching converter components (inductors, flywheel diodes and filtering capacitors) should also be as short and wide as possible. The electrical loops that these components form should be as small and compact as possible, with the ground referenced components forming a star connection.

Due to the fast switching transitions appearing on the sixteen reset OUTx pins, it is recommended to keep these traces as short as possible. Also, to minimize potential cross-talk between outputs, it is advisable to maintain as much clearance between each of the output traces.

Grounding Guidelines

The PWB should have an internal ground plane that extends under the DLPA200. All 9 ground pins (1, 7, 14, 20, 41, 46, 53, 55, and 60) must be connected to the ground plane using the shortest possible runs and vias. All filter and bypass capacitors must be placed near the pin being filtered or bypassed for the shortest possible runs to the part and to the ground plane.

Thermal Guidelines

The DLPA200 package should be thermally bonded or soldered to an external thermal pad on the PWB surface. The recommended dimensions of the thermal pad are 10 x 10 mm centered under the part. The metal bottom of the package is tied internally to the substrate at the VRESET_RAIL voltage level. Therefore, the thermal pad on the board must be isolated from any other extraneous circuit or ground and no circuit vias are allowed inside the pad area. Thermal pads are required on both sides of the PWB and should be connected together through an array of 5 x 5 thermal vias, 0.5 mm in diameter. **Thermal pads and the thermal vias are connected to VRESET_RAIL and isolated from ground, or any other circuit.** An internal P12V or VBB plane should be located directly underneath the top layer and have an isolated area under the DLPA200. This isolated area must be a minimum of 20 cm^2 and connect to the thermal pad of the DLPA200 through the thermal vias. The potential of the isolated area will also be at VRESET_RAIL. The internal ground plane should extend under the DLPA200 to help carry the heat away. Please refer to the PowerPAD Thermally Enhanced Package application report (TI literature number SLMA002) for details on thermally efficient package design considerations.

Careful consideration should be taken with respect to DLPA200 placement in the vicinity of local PWB hotspots. Heat generated from adjacent components may impact the DLPA200 thermal characteristics.

Power Supply Rail Guidelines

Table 5 through Table 9 provides discrete component selection guidelines.

The P12V filter and bypass capacitors should be distributed and connected to pin 11 and pins 48 & 50. These capacitors should be placed as near to their respective pins as possible and if necessary, should be placed on the bottom layer.

The V5REG filter and bypass capacitors must be placed near and connected to pin 47.

The VBIAS_RAIL etch runs should be routed in the following order: pin 40, pin 31, pin 30, pin 21, pin 80, pin 71, pin 70, and pin 61. The etch runs should be short and direct as they must carry 35 ns current spikes of up to 0.64 amps peak. Bypass capacitors should be located near and connected to pins 30 and 71 to provide bypassing on both sides.

The VBIAS_LHI filter and bypass capacitors must be placed near and connected to pin 10.

The VBIAS filter and bypass capacitors must be placed near and connected to pin 9. VBIAS pin 9 must also be connected (optionally with a 0-ohm resistor) to VBIAS_RAIL at or between pins 21 and 80.

The VRESET_RAIL etch runs should be routed in the following order: pin 36, pin 35, pin 26, pin 25, pin 76, pin 75, pin 66, and pin 65. The etch runs should be short and direct as they must carry 35 ns current spikes of up to 0.64 amps peak. Bypass capacitors should be placed near and connected to pins 35 and 66 to provide bypassing on both sides.

The VRESET filter and bypass capacitors must be located near and connected to pin 13. VRESET pin 13 must also be connected (optionally with a 0-ohm resistor) to VRESET_RAIL at or between pins 25 and 76.

The VOFFSET_RAIL etch runs should be routed in the following order: pin 23, pin 28, pin 33, pin 38, pin 63, pin 68, pin 73, and pin 78. The etch runs should be short and direct as they must carry 35 ns current spikes of up to 0.64 amps peak. Bypass capacitors should be placed near and connected to pins 28 and 73 to provide bypassing on both sides.

The VOFFSET filter and bypass capacitors must be placed near and connected to pin 49. VOFFSET pin 49 must also be connected (optionally with a 0-ohm resistor) to VOFFSET_RAIL at or between pins 38 and 63.

NOTE

Aluminum electrolytic capacitors may not be suitable for the DLPA200 application. At the switching frequencies used in the DLPA200 (up to 1.5MHz), aluminum electrolytic capacitors drop significantly in capacitance and increase in ESR resulting in voltage spikes on the power supply rails, which could cause the device to shut down or perform in an unreliable manner.

COMPONENT SELECTION GUIDELINES

Table 5. 5-V Regulator

COMPONENT	VALUE	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
P12V filter capacitor	10 to 33 µF, 20 VDC, 1Ω max ESR	Tantalum or ceramic	Pos: P12V, pin 11 (locate near pin 11)	Neg: Ground
P12V bypass capacitor	0.1 µF, 50 VDC, 0.1Ω max ESR	Ceramic	P12V, pin 11 (locate near pin 11)	Ground
V5REG filter capacitor	0.1 (1) to 1.0 µF, 10 VDC, 2.5Ω max ESR	Tantalum or ceramic	Pos: V5REG, pin 47 (locate near pin 47)	Neg: Ground
V5REG bypass capacitor	0.1 µF(1), 16 VDC, 0.1Ω max ESR	Ceramic	V5REG, pin 47 (locate near pin 47)	Ground

(1) To ensure stability of the linear regulator, the capacitance should not be less than 0.1 µF.

Table 6. Bias Voltage Boost Converter

COMPONENT	VALUE	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
LHI filter capacitor	10 µF, 20 VDC, 1Ω max ESR	Tantalum or ceramic	Pos: VBIAS_LHI, pin 10 (locate near pin 10)	Neg: Ground
LHI bypass capacitor	0.1 µF, 50 VDC, 0.1Ω max ESR	Ceramic	VBIAS_LHI, pin 10 (locate near pin 10)	Ground
VBIAS filter capacitor	1 to 10 µF, 35 VDC, 1Ω max ESR; (3.3 µF nominal value)	Tantalum or ceramic	Pos: VBIAS, pin 9 (locate near pin 9)	Neg: Ground
VBIAS bypass capacitor	0.1 µF, 50 VDC, 0.1Ω max ESR	Ceramic	VBIAS, pin 9 (locate near pin 9)	Ground
VBIAS_RAIL bypass capacitors (2 required)	0.1 µF, 50 VDC, 0.1Ω max ESR	Ceramic	VBIAS_RAIL, pins 30 and 71 (locate near pins 30 and 71)	Ground
Resistor jumper (optional)	0-Ω normally (1Ω for testing(1))		VBIAS, pin 9	VBIAS_RAIL, pins 21 or 80
Inductor	22 µH, 0.5 amp, 160 mΩ ESR	Coil Craft DT1608C-223 (or equivalent)	VBIAS_LHI, pin 10	VBIAS_SWL, pin 8
Schottky diode	0.5A, 40V (minimum)	Motorola MBR0540T1 or STMicroelectronics STPS0540Z, STPS0560Z (or equivalent)	Anode: VBIAS_SWL, pin 8	Cathode: VBIAS, pin 9

(1) Allows for VBIAS current measurement.

Table 7. Reset Voltage Boost Converter

COMPONENT	VALUE	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
VRESET filter capacitor	1 to 10 µF, 35 VDC, 1Ω max ESR; (3.3 µF nominal value)	Tantalum or ceramic	Neg: VRESET, pin 13 (locate near pin 13)	Pos: Ground
VRESET bypass capacitor	0.1 µF, 50 VDC, 0.1Ω max ESR	Ceramic	VRESET, pin 13 (locate near pin 13)	Ground
VRESET_RAIL bypass capacitors (2 required)	0.1 µF, 50 VDC, 0.1Ω max ESR	Ceramic	VRESET_RAIL, pins 35 and 66 (locate near pins 35 and 66)	Ground
Resistor jumper (optional)	0-Ω normally (1Ω for testing(1))		VRESET, pin 13	VRESET_RAIL, pins 25 or 76
Inductor	22 µH, 0.5A, 160 mΩ	Coil Craft DT1608C-223 (or equivalent)	VRESET_SWL, pin 12	Ground

(1) Allows for VRESET current measurement.

Table 7. Reset Voltage Boost Converter (continued)

COMPONENT	VALUE	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
Schottky diode	0.5 A (minimum), 60 V	STMicroelectronics STPS0560Z or International Rectifier 10MQ060N (or equivalent)	Cathode: VRESET_SWL, pin 12	Anode: VRESET, pin 13

Table 8. Offset Voltage Regulator

COMPONENT	VALUE	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
VOFFSET/VCC2 filter capacitors (2 required)	1 (1) to 4.7 (2) µF, 35 VDC, 1Ω max ESR	Tantalum or ceramic	Pos: VOFFSET, pin 49 (1st near pin 49) Pos: DMDVCC2 pins (locate 2nd at DMD)	Neg: Ground at DLPA200 Neg: Ground at DMD
VOFFSET/VCC2 bypass capacitors (5 required)	0.1 µF, 50 VDC, 0.1Ω max ESR	Ceramic	VOFFSET, pin 49 (locate 1 near pin 49) DMD DMDVCC2 pins (locate 4 near DMD pins)	Ground at DLPA200 Ground at DMD
VOFFSET_RAIL bypass capacitor (2 required)	0.1 µF, 50 VDC, 0.1Ω max ESR	Ceramic	VOFFSET_RAIL, pins 28 and 73 (locate near pins 28 and 73)	Ground
Resistor jumper (optional)	0-Ω normal (1Ω for testing (3))		VOFFSET, pin 49	VOFFSET_RAIL, pins 38 or 63
Resistor jumper (optional)	0-ohm normal (1Ω for testing (4))		VOFFSET, pin 49	DMDVCC2 pins

(1) To ensure stability of the linear regulator, the absolute minimum output capacitance should not be less than 1.0 µF.
(2) Recommended value is 3.3 µF each. Different values are acceptable, provided that the sum of the two is 6.8 µF maximum.
(3) Allows for V_{OFFSET} current measurement
(4) Allows for DMDVCC2 current measurement

Table 9. Pullup Resistors

COMPONENT	VALUE	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
Resistor	1 kΩ		SCPDO, pin 42	Chipset controller 3.3-V V_{DD}
Resistor	1 kΩ		$\overline{IRQ}$, pin 43	Chipset Controller 3.3-V V_{DD}
Resistor (optional)	1 kΩ		$\overline{OE}$, pin 6	Chipset Controller 3.3-V V_{DD}

REVISION HISTORY

Changes from Original (April 2010) to Revision A **Page**

- Changed device marking to include TI internal part number 5

Changes from Revision A (June 2010) to Revision B **Page**

- Added APPLICATIONS 1
- Changed the DESCRIPTION, added Table 1 1
- Added *Device Configurations* table 3
- Changed I/O type of the signals 6
- Corrected VRESET_SWL, VBIAS_RAIL and VOFFSET_RAIL signal notations 7
- Added V_{BIAS} voltage to ELECTRICAL CHARACTERISTICS 9
- Added V_{RESET} voltage values to Reset Voltage Buck-Boost Converter 9
- Added V_{OFFSET} voltage to ELECTRICAL CHARACTERISTICS 10
- Added subsection *Serial Communications Port (SCP)* 14
- Deleted Driver Output Logic Block section 14
- Added *Serial Communications Port Signal Definitions* table 15
- Changed Warning to Caution 15
- Changed Warning to Note 16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DLPA200PFC	ACTIVE	TQFP	PFC	80	5	Pb-Free (RoHS)	Call TI	Level-2-260C-1 YEAR	

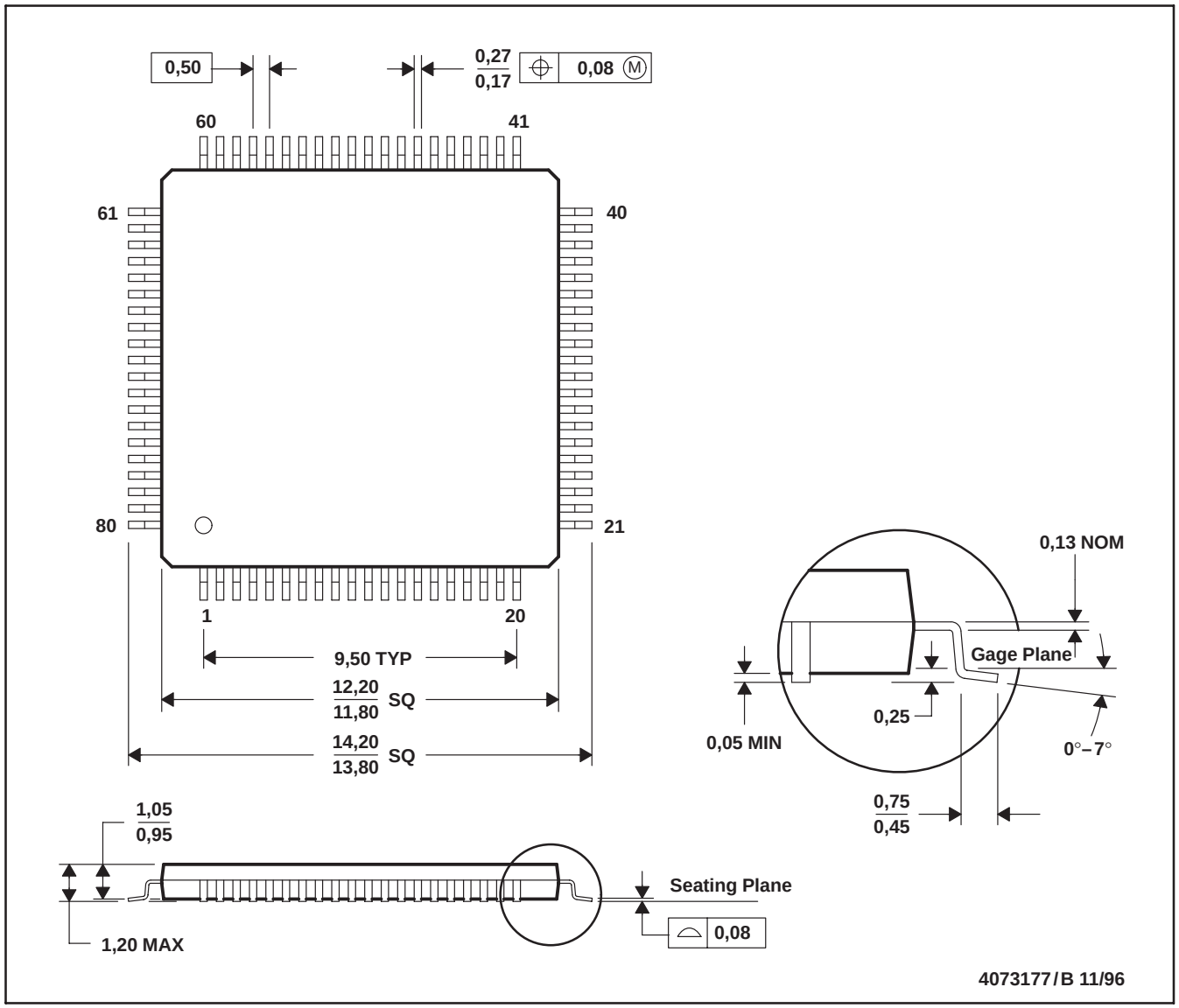
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MTQF009A – OCTOBER 1994 – REVISED DECEMBER 1996

PFC (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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